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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,336	11/13/2001	Chaitanya S. Rajguru	10559-519001 / P12423	5776

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EXAMINER	
DESTA, ELIAS	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/993,336	RAJGURU, CHAITANYA S.	
	Examiner	Art Unit	
	Elias Desta	2857	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 04 November 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☒ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

8. ☒ The drawing correction filed on *17 July 2003* is a)☒ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

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Continuation of 5. does NOT place the application in condition for allowance because: The amended claims are incorporating the canceled dependent claims limitation without including any distinguishing elements from the previous argument.

The Examiner believes that in reference to claim 1, 7, 13, 19 and 20: as discussed in Kawahara et al., Fig. 1 and page 127, paragraph 2 provides a means to measure an actual capacity of the charge pump and to reset the capacity of the charge pump to a value based on the measured capacity. Further, the system implements an accurate reference voltage, which provides a means to control the values of the charge pump capacity.

Kawahara et al. provides two charge pump voltages (VH and VP) to control the programming and erasing speed of the flash memory (see Kawahara et al., page 127, 1st column and 2nd paragraph). These voltages are controlled using a reference voltage to achieve the required value (see page 127, 2nd column, 3rd paragraph). Also Kawahara et al. in Fig. 1 shows that the output of the charge pumps is measured in pico farad (pF) (see page 127, 1st column, 1st paragraph, starting 3rd line). In Fig. 6(a), the charge pump is provided with a measuring circuit that enables the system to monitor the charge pump based the reference voltage because the reference voltage is connected to CR of known value. The capacitance value, as discussed in page 131, 1st column, 1st paragraph is used to reset the capacity of the charge pump to a known reference value because Kawahara et al. teaches that doing so guarantees the accurate control of the voltage to the charge pump.

Fig. 1 has the same high level schematic as Fig. 1 of the claimed invention, and both figures don't get into a characterization of feedback loop arrangement. However, Kawahara et al. uses a reference feedback mechanism to control the large and medium charge pump output to the memory cells because the voltage and temperature compensation as discussed in page 129, 1st column and 1st & 2nd paragraphs can only achieved when the compensated values are evaluated against the output of the signals gathered at VP and VP output in order to control and improve the read and write times required by the flash memory.